IN THE SPECIFICATION:

Kindly replace the paragraph beginning at page 1, line 29 with the following:

Generally speaking the ISI can be divided into two components, namely precursor and post cursor ISI. Conventionally a feedforward equalizer (FFE) attempts to remove precursor ISI, and decision feedback equalization (DFE) attempts to remove postcursor ISI. Fig. 1 is illustrative of a conventional feedforward equalizer used in conjunction with decision feedback equalizer in a data communications channel. As shown in Fig. 1, an analog, input signal from a communication channel is converted ~~by~~ to a digital signal by analog-to-digital converter 102. The digital signal is processed by FFE 104 and DFE ~~106~~ 105 in a conventional manner. DFE ~~106~~ 105 comprises decision circuit 108 and feedback filter 110. Examples of conventional arrangements are discussed in U.S. Patent Nos. 5,513,216 and 5,604,769, the contents of each of which are incorporated herein by reference.

Kindly replace the paragraph beginning at page 7, line 26 with the following:

Reference is now made to Fig. 3 which shows a block diagram of a feedforward equalizer implemented as a high-pass filter used in conjunction with a decision feedback equalizer in accordance with a first embodiment of the present invention. As shown therein, an analog input signal is converted to a digital signal by analog-to-digital converter (ADC) ~~312~~ 302. The FFE 304 processes the digitized input signal to effectively cancel the precursor ISI and shorten the length of the postcursor ISI. Fig. 4 illustratively shows the shorten length of the postcursor ISI of when an input signal is processed by FFE 304 of the present invention. FFE 304 is preferably implemented as a high-pass filter to shorten the tail. The output of FFE 304 is then processed by DFE 305 to effectively cancel the postcursor ISI in a known manner. DFE 305 comprises decision circuit 308 and feedback filter 310. Decision circuit 308 may be implemented by, for example, a threshold circuit, a Viterbi detector or the like. Feedback filter 310 is preferably implemented as a FIR filter.

Kindly replace the paragraph beginning at page 9, line 16 with the following:

Fig. 8 shows a more detailed schematic of an adaptive FIR filter for FFE. As shown therein, the main tap W_0 is kept at its initial value and is not adapted. Coefficients $W_{-m} \ldots W_{-1}$ can be determined by LMS engines ~~840$_m$~~ 840$_{-m}$ ... 840$_{-1}$ in accordance with a least mean square (LMS) algorithm based on gradient optimization. The change in tap weight coefficients ΔWn is calculated to be $\Delta Wn = \Delta * Xn * En$; where Δ is the adaptation rate and E is the error output by the error generator 724. Coefficients $W_1 \ldots W_n$ are similarly determined by LMS engines $840_1 \ldots 840_n$. In addition limiters $830_1 \ldots 830_n$ are provided to enforce the constraints discussed above.

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